01-091
1496.00113

TRIPLE CONVERSION RF TUNER WITH SYNCHRONOUS LOCAL OSCILLATORS

Cross Reference to Related Applications

The present application may relate to co-pending application Serial No. _____ (Attorney Docket No. 1496.00114), filed concurrently, which is each hereby incorporated by reference in its entirety.

Field of the Invention

The present invention relates to a method and/or architecture for a radio frequency (RF) tuner generally and, more particularly, to a television tuner architecture that is amenable to higher integration and lower cost while maintaining excellent performance for both cable and broadcast systems.

Background of the Invention

Referring to FIG. 1, a current single conversion tuner module 10 is shown. Single conversion refers to the number of frequency translations that the incoming signal is subjected. For example, in the U.S. the frequency plan for most cable networks

span the frequencies from 54MHz to 857MHz. Each channel at the input of the tuner 10 spans 6MHz for a total of 133 input channels. The tuner 10 selects one out of the multitude of channels and translates the selected channel to a fixed IF frequency of 44MHz. Frequency translation is also commonly termed as conversion, hence the tuner 10 is often referred to as a single conversion system. The single conversion is achieved by mixing the incoming signals with a local oscillator signal (OSC) present inside the tuner 10. For example, if an incoming channel centered at 100MHz is mixed with a 144MHz local oscillator signal, the resultant signal at the output of the mixer 14 is a sum frequency product at 244MHz and a difference frequency product at 44MHz. The sum frequency product is typically eliminated by use of a SAW filter 16, centered at the desired output or Intermediate Frequency (IF), in this case at 44MHz. SAW filters provide a high degree of selectivity to the incoming signals providing a significant level of attenuation to signals outside of the pass band. In the U.S., the SAW filter pass band is selected to be approximately one channel bandwidth (i.e., 6MHz).

If in the above illustration, the channel at 100MHz is defined as the desired channel, there also exists an image or

undesired channel which could also mix with the local oscillator signal OSC and produce an output at the IF of 44MHz. Consider an example of a channel at 188MHz. If the channel were to be mixed with a local oscillator signal at 144MHz, the channel could also produce a difference output at the IF of 44MHz and a sum frequency output product at 188MHz. The SAW filter 16 would attenuate the output at 188MHz. However, the SAW filter 16 would not be able to distinguish between the output of the image channel mixing and the output of the desired channel mixing, both of which would be at the desired IF of 44MHz. The single conversion tuner 10 overcomes an undesired channel by the use of the tracking channel filter 12 at the input of the tuner 10. The incoming signals pass through the tracking filter 12 before the mixer 14. Tracking filters are typically 20-40MHz wide and eliminate the undesired image channel from being subjected to the mixing process, thereby ensuring that the output at the IF is only due to that of the desired channel.

For a given mixing step, there exists an undesired image channel spaced at twice the IF from the desired channel. While the use of input tracking filters greatly alleviates the image channel problem, input filters need to track the local oscillator frequency in order to ensure that the image rejection is maintained across

the input signal band. Moreover, in cable modem systems, for proper operation each modem also needs to present a controlled input impedance across the input frequency band. The input tracking filters present a non-uniform input impedance across the input frequency range while attenuating the image channel. Typically, input tacking filters have tuned passive devices, which need to be manually tuned during the tuner module assembly process. Manual tuning is a significant portion of the manufacturing costs. To overcome the single conversion tuner drawbacks, tuner manufacturers have introduced tuner modules, which feature a dual conversion architecture.

Referring to FIG. 2, a typical dual conversion tuner module 20 is shown. In dual conversion tuners the frequency translation from the input frequency band of 48MHz-857MHz to the output IF of 44MHz is achieved in two mixing steps. Nominally the first mixing step 24 involves upconverting the entire input frequency band to a first IF frequency (IF1) which is 1100MHz. There are two desirable properties associated with this upconversion mixing. The first IF at 1100MHz is out of band to the input channel frequency band. Also, the image channel for the first IF needs to be filtered out with a fixed low pass filter 22

at the input of the tuner 20. The low pass filter 22 would not have to be a tracking filter and could help present a controlled impedance to a cable network. If for example, the desired channel is located at 100MHz, the first local oscillator signal frequency (OSC1) would have to be 1200MHz for a subtractive upcoversion mixing step for a first IF of 1100MHz. Since the tuner module 20 still has to have an output at 44MHz, the second mixing step 28 downcoverts the signal at the first IF by mixing it with a second local oscillator signal (OSC2) at a frequency of 1056MHz.

As in the single conversion tuner 10, there exists a SAW filter 30, which provides the desired channel selectivity at 44MHz. However, the dual conversion tuner architecture has the following drawback. The image channel for the second mixing step 28 could still be present at the first IF output IF1. For example, in the above illustration if there is a signal present at the first IF IF1 at 1012MHz, the signal too would downconvert and appear at the second IF output IF2 at 44MHz. The SAW filter 30 would not be able to distinguish such a signal from the desired channel. Therefore, the filter 26 at the first IF of 1100MHz should have a narrow pass band or a high enough Q (quality factor) to suppress the signal at the image frequency of the second mixing process. Typically the Q

would have to be about 50 to ensure sufficient attenuation of the image. Such a narrowband filter at high frequencies such as 1100MHz are expensive and often necessitate the use of a matching network to properly interface to both the output of the first mixer 24 and to the input of the second mixer 28.

Since the dual conversion architecture 20 employs two mixing steps, there could be additional distortion and phase noise compared to the single conversion tuner architecture 10. Each mixing step could introduce distortion due to the mixing process. The phase noise present in the local oscillator signal(s) could also degrade the signal integrity.

Summary of the Invention

The present invention concerns an apparatus comprising a first circuit, a second circuit and a third circuit. The first circuit may be configured to generate an upconverted signal in response to an input signal and a first oscillation signal. The second circuit may be configured to generate a downconverted signal in response to the upconverted signal and as second oscillation signal. The third circuit may be configured to generate an output signal in response to the downconverted signal and a third

oscillation signal derived from the second oscillation signal. The upconverting and downconverting may filter undesired channels from the output signal.

The objects, features and advantages of the present invention include providing a method and/or architecture for a RF tuner that may (i) provide selectivity and gain while not degrading the quality of the incoming signal by adding unwanted noise or distortion, (ii) implement a tuner with higher levels of integration, thereby reducing the number of passive components required, and reduce tuner form factor, and/or (iii) eliminate the need for manually tuned components providing increased reliability of operation.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a conventional single conversion tuner circuit;

FIG. 2 is a block diagram of a conventional dual conversion tuner circuit;

FIG. 3 is a block diagram of a preferred embodiment of the present invention; and

FIG. 4 is a detailed block diagram of the circuit of FIG. 3.

Detailed Description of the Preferred Embodiments

Referring to FIG. 3, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented as a triple conversion RF tuner with synchronous local oscillators. The present invention may provide a tuner with higher levels of integration, thereby reducing the number of passive components required. The present invention may also reduce tuner form factor. In addition, the present invention may eliminate the need for manually tuned components providing increased reliability of operation.

The circuit 100 generally comprises a circuit 102, a circuit 104 and a circuit 106. The circuits 102 and 106 may be conversion circuits. The circuit 104 may be a logic and conversion circuit. The circuit 102 may have an input 110 that may receive input signal (e.g., INPUT), an input 112 that may receive a clock

signal (e.g., OSC1) and an output 114 that may present a signal (e.g., IF1'). The signal INPUT may be an input frequency band. The circuit 104 may have an input 120 that may receive the signal IF1' an input 121 that may receive a signal (e.g., OSC2), an output 122 that may present a signal (e.g., OSC3_IN_PH), an output 124 that may present a signal (e.g., IF2') and an output 126 that may present a signal (e.g., OSC3_QUAD). The circuit 106 may have an input 130 that may receive the signal OSC3_IN_PH, an input 132 that may receive the signal RF2', an input 134 that may receive the signal OSC3_QUAD, and an output 136 that may present an output signal (e.g., OUTPUT). Each of the oscillator signals OSC1, OSC2, and OSC3 may be implemented as a periodic wave signal (e.g., sinusoidal, square, triangle, etc.).

Referring to FIG. 4, a more detailed diagram of the circuit 100 is shown. The circuit 102 is shown comprising a circuit 160, a circuit 162 and a circuit 164. The circuit 160 may be implemented as a low noise amplifier (LNA) circuit. The circuit 162 may be implemented as a mixer circuit. The circuit 164 may be implemented as an intermediate filter circuit.

The circuit 104 may have an input 121a that may receive an in-phase portion of the signal OSC2 (e.g., OSC2_IN-PH) and an

input 121b that may receive a quadrature portion of the signal OSC2 (e.g., OSC2_QUAD). The circuit 104 generally comprises a circuit 170, a circuit 172, a circuit 174, a circuit 176, a circuit 178 and a circuit 180. The circuit 170 may be implemented as a mixer circuit. The circuit 172 may be implemented as a divider circuit. The circuit 174 may be implemented as a summation circuit. The circuit 176 may be implemented as an intermediate filter circuit. The circuit 178 may be implemented as a mixer circuit. The circuit 180 may be implemented as a divider circuit.

The circuit 106 generally comprises a circuit 190, a circuit 192, a circuit 194 and a circuit 196. The circuit 190 may be implemented as a mixer circuit. The circuit 192 may be implemented as a mixer circuit. The circuit 194 may be implemented as a summation circuit. The circuit 196 may be implemented as an implementation filter circuit. In one example, the circuit 196 may be implemented as a SAW filter.

The input frequency band signal INPUT may be passed through the variable gain low noise amplifier 160. The amplifier 160 may condition the amplitude of signal INPUT such that the strength of the signal INPUT presented to the mixer 162 is relatively constant even with varying amplitudes of the signal

INPUT. The mixer 162 may upconvert the entire input signal band to a first IF of 1324MHz. A first local oscillator frequency (e.g., OSC1) may be variable over a frequency of 1378MHz-2324MHz. For example, if the desired channel is at 100MHz, the chosen first frequency OSC1 may be 1424MHz which generally implies that the image channel for the mixer 162 may be located at 2748MHz (which is out of band to the channel frequencies present on a cable network). After the filter 164 operation, the mixers 170 and 178 may downconvert the input signal to the second IF (filter 176) at 300MHz.

A local oscillator clock (e.g., OSC2_IW_PH) to the mixers 170 and 178 may be at 1024MHz, which implies that the image channel for the mixers 170 and 178 may be located at 724MHz. The filter 176 may eliminate or substantially attenuate signal content at 724MHz, which is possible to achieve with a filter Q of about 20. Such a filter considerably reduces the performance needed for implementing the filter 176 when compared to the filter in the dual conversion tuner architecture 20 of the background section. In addition, a filter with Q of around 20 could be achieved by low cost passive components and also lends to being integrated onto the same integrated circuit as the mixer 162.

To further improve the image rejection capability, the mixers 170 and 178 may be implemented as an image reject type filter. The input signal may be mixed in two separate signal paths, with the local oscillator clocks OSC2_IW_PH and OSC2_QUAD phased in quadrature relationship in the two paths. A quadrature relationship may allow the signals OSC2_IW_PH and OSC2_QUAD to be phased 90 degree apart in the two signal paths. After the quadrature mixing process (e.g., the mixers 170 and 178), each of the two signal paths may be combined at the summation circuit 174 and filtered at the filter 176 to form the signal IF2'. A more detailed explanation can be found in co-pending application Serial No. _____ (Attorney Docket No. 1496.00114). The mixers 190 and 192 may then downcovert the IF2' signal to 44MHz, by mixing with the third local oscillator signals OSC3_IW_PH and OSC3_QUAD located at a frequency of 256MHz.

The mixers 190 and 192 may also be implemented as an image reject type mixers that may attenuate the image signals for the mixing step 190 and 192, which may be located at 212MHz. Hence, the requirement on the filter 176 may be to provide attenuation of signal energy present at 212MHz which is possible with a filter Q of around 20. Similar to the filter 164, the

filter 176 may also be implemented with low-cost passive components or integrated onto the same integrated circuit as the mixers 170 and 178. The quadrature outputs of the third mixing step 190 and 192 may be combined at the summation circuit 194 and then filtered by the SAW filter 196 at 44MHz to provide the desired channel selectivity. The triple conversion architecture 100 may provide high performance and high Q filter.

To help ensure that the additional mixing step in the present architecture does not degrade the signal integrity by introducing additional phase noise due to the third signal OSC3, the architecture generally exploits the frequency relationship between OSC2 and OSC3 (e.g., OSC2 may be 4 times the frequency of OSC3). Such division may be achieved by dividing the frequency of OSC2 by four, since a synchronous frequency division process may improve the signal phase noise by 20log(4), or about 12dB. The synchronous division process 172 and 180 may ensure that the phase noise of OSC3 is 12dB lower than that of OSC2. The circuit 100 does not generally degrade the tuner signal integrity by the addition of the third mixing step 190 and 192.

The circuit 100 may be implemented as a triple conversion tuner circuit that may overcome the drawbacks of the conventional

dual conversion circuit and may be enabled either as a low cost, small form factor solution or alternatively integrated onto an Integrated Circuit (IC). The circuit 100 may also be implemented without introducing additional phase noise into the tuner signal path when compared to a conventional dual conversion architecture.

The present invention may be applicable in tuners for cable modems, analog TVs, PC-TVs, set-top boxes or in tuners for TV signal reception. In one example, the circuit 100 may be implemented as a single microcircuit (or microchip) integrating all the active elements such as the LNA, the mixers, the combiners, the local oscillator generating circuits and any additional signal amplification circuits or distributed onto separate integrated circuits. However, the circuit 100 may be implemented on a plurality of microcircuits (or microchips) as needed to meet the design criteria of a particular implementation.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.